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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
SCS-550-489	

Application Number	Filed
10/715,368	November 19, 2003
First Named Inventor: FLYNN	
Art Unit: 2116	Examiner: M. Brown

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

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November 26, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

STATEMENT OF ARGUMENTS IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

Error #1. The Examiner ignores the limitations of independent claims 1, 6 and 11

Each of independent claims 1, 6 and 11 specifies that the "at least one further circuit" has an interrelationship with the processor so as to support "data processing of said processor at **at least one intermediate data processing performance level**" (emphasis added). In the Final Rejection, page 3, lines 10-12, the Examiner admits that the Cooper reference fails to disclose the claimed "at least one further circuit." However, in the admission, the Examiner omits a significant portion of each of the independent claims, i.e., the portion stating an interrelationship in which the data processing is supported by the further circuit at "at least one intermediate data processing performance level" during the change from a first desired data processing performance level to a second desired data processing performance level. The Examiner's failure to appreciate that Applicant's independent claims 1, 6 and 11 all positively recite this interrelationship is clear evidence of error on the Examiner's part in his attempt to read prior art on the pending claims.

Moreover, it is noted that the Examiner's admission (that Cooper fails to contain the disclosure) is immediately after the Examiner's representation that Cooper discloses a first performance level in the "low power state, see column 5, lines 35-36" changing to a second performance level "high power state, see column 5, line 36." In spite of the subsequent admission, the Examiner appears to suggest that, during the change from low to high, Cooper teaches operation "at said at least one intermediate data processing level during said change" with a reference to "column 5, lines 33-42 and column 8, lines 6-9." Given the contradictory language, it is not clear whether the Examiner believes the "at least one further circuit" of claims 1, 6 and 11 is taught by the Cooper reference or whether his admission that Cooper fails to teach the at least one further circuit is the Examiner's position.

It has been Applicant's position throughout the consideration and response to the four previous Official Actions that Cooper does not teach any "intermediate data processing performance level." A review of the Examiner's cited portion of the Cooper reference will indicate that Cooper specifically recites "performance control logic 16 that ensures that processor 12 is in a relatively quiescent state by intercepting all interrupts." Applicant previously made of record the Webster's dictionary definition of "quiescent" which is "marked by inactivity or repose: tranquilly at rest." Thus, given the ordinary definition of the word "quiescent," the Examiner's apparent suggestion that this is "at least one intermediate data processing performance level" is the direct opposite of such quiescence.

The Examiner in the Final Rejection, apart from his self-contradiction between suggesting that Cooper teaches the at least one intermediate data processing performance level and his admission that Cooper fails to disclose the at least one intermediate data processing performance level, ignores the fact that Cooper actually teaches "quiescence" between performance states (Cooper actually states "processor 12 is limited to switching performance states only during relatively quiescent states." Column 5, lines 17-18).

Error #2. The Examiner misunderstands the Kobayashi reference teaching

Kobayashi teaches an operating data processing machine and a back-up data processing machine (abstract, lines 1-2). The Examiner seems to be suggesting that Kobayashi's teaching of a main processor which incurs a failure and is inoperative is somehow Applicant's claimed "intermediate processing level" which then results in operation of the Kobayashi back-up data processing machine.

However, Kobayashi has no disclosure of any intermediate data processing level, whether "quiescent" as disclosed in Cooper or inoperative "when a failure occurs" in the Kobayashi reference. How or where the Examiner believes either Cooper or Kobayashi teach Applicant's claimed at least

one further circuit and its interrelationship with the processor during changes in desired data processing performance levels is not seen.

The Examiner is respectfully requested to identify any "intermediate data processing performance level" is disclosed in either of the Cooper or Kobayashi references. Without the disclosure of this claimed interrelationship, there is no support for any *prima facie* case of obviousness of claims 1-11 under 35 USC §103 over Cooper in view of Kobayashi.

Error #3. The Examiner errs in his argued teaching of the combination of Cooper and Kobayashi

The Examiner appears to allege that the combination of the Cooper and Kobayashi references would somehow provide Applicant's claimed invention. It is clear that Cooper teaches changing performance levels "only during relatively quiescent states" as noted above, while Kobayashi does not change data processor performance levels and merely substitutes a back-up data processing during failure of the primary data processor.

If these references were somehow combined, one of ordinary skill in the art would have to make a decision as to whether he is going to use the single data processor of Cooper or the two data processors of Kobayashi (with one being designated as a back-up). Even if one did attempt to combine these two disclosures in the manner suggested by the Examiner, in addition to making the decision as to how many data processors are to be utilized, one of ordinary skill in the art would also have to ignore the Cooper teaching of power switching only during the "quiescent" state and also ignore the Kobayashi teaching of switching processors when the primary processor is inoperative, i.e., after "a failure occurs."

Thus, the Examiner has failed to indicate how the combination of the Cooper and Kobayashi references would render obvious Applicant's independent claims 1, 6 and 11 and therefore has failed to meet the burden of establishing a *prima facie* case of obviousness.

Error #4. The Examiner fails to provide any "reason" or "motivation" for combining Cooper and Kobayashi

In accordance with the recent Supreme Court decision in *KSR v. Teleflex,* it is incumbent upon the Examiner to articulate some "reason" for picking and choosing elements from the various prior art references and then combining them in the manner of the claimed invention. The Supreme Court specifically indicated that the examiner's rationale must be made explicit ("to facilitate review, this analysis should be made explicit." *KSR International Co. v. Teleflex, Inc.* 82 USPQ2d 1385, 1396 (SCT 2007)).

The only statement purporting to be a reason or motivation is the Examiner's conclusion that one would want to "assure that data being processed and data concerning the failure are dumped to an auxiliary memory to facilitate analysis of the failures." This motivation assumes that one wishes to change processors as in Kobayshi rather than merely change processor performance level as in the single processor of Cooper. Which does one do and why? Again, the Examiner has provided selective rationale based only upon Applicant's independent claims and the information contained in Applicant's specification.

Nowhere does the Examiner indicate that either Cooper or Kobayashi appreciates that there is a problem of energy consumed by a data processing system which problem is solved by the presently claimed invention. The Examiner's combination of Cooper and Kobayashi would not reduce energy consumption. Kobayashi's back-up processor would require as much energy as the primary processor and perhaps even more (in view of the admitted additional processing necessary to save information and data concerning the failure to an auxiliary memory to facilitate analysis).

Because the Examiner has failed to provide any reason for combining the Cooper and Kobayashi references, he has failed to establish a *prima facie* case of obviousness under 35 USC §103 with respect to independent claims 1, 6 and 11.

Error #5. The Examiner appears to ignore the fact that both Cooper and Kobayashi teach away from Applicant's claimed combination

As noted above, the Cooper reference clearly teaches away from Applicant's claimed "intermediate data processing performance level" by teaching that performance levels must be in "a relatively quiescent state." Kobayashi does not teach changing performance level at all, but rather, teaches changing data processors, but only when the primary processor is inoperative, i.e., no intermediate performance level. Both Cooper and Kobayashi teach either "quiescent" operation of a single processor when changing processing performance levels or inactive data processing occurring when Kobayashi's primary processor fails and prior to the back-up processor beginning operation.

Because both Cooper and Kobayashi references lead one of ordinary skill in the art away from the claimed invention, this is a complete rebuttal of any *prima facie* case of obviousness established by the Examiner.

SUMMARY

Independent apparatus claim 1, method claim 6 and means-plus-function claim 11 all require a specific interrelationship between the "one further circuit" and the "processor." Cooper's teaching of a single processor going to a "quiescent" state while changing power levels and Kobayashi's teaching of "inoperative" data processing when changing processors fails to disclose any "intermediate level of data processing" and would lead one of ordinary skill in the art away from the claimed invention.

As a result of the above, there is simply no support for the rejection of Applicant's independent claims 1, 6 and 11 or claims dependent thereon under 35 USC §103. Applicant respectfully requests that the Pre-Appeal Panel find that the application is allowed on the existing claims and prosecution on the merits should be closed.